**PVP 14**

Code: EC5T5

**III B.Tech - I Semester – Regular/Supplementary Examinations**
**October 2018**

# DIGITAL IC APPLICATIONS
## (ELECTRONICS AND COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Write the structural program for an AND gate Verilog HDL.
b) What is the difference between net delay and gate delay?
c) Explain logic levels of CMOS Logic?
d) What do you mean by multiple emitter transistor used in TTL?
e) In terms of power consumption compare CMOS with TTL.
f) Design an NAND gate using 2x1 Multiplexer.
g) Draw the truth table of seven segment Decoder.
h) Draw the state table of Ring Counter.
i) Convert J-K flipflop to D flip-flop with enable input.
j) What is EEPROM?
k) Explain two dimensional decoding in ROM memory?

## PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Design 8X1 MUX using two 4X1 MUX and one 2X1 MUX and implement the same in Verilog HDL. 10 M

   b) Explain non-blocking assignments with proper example. 6 M

3. a) What is interfacing? Explain interfacing between low voltage TTL to low voltage CMOS logic. 10 M

   b) Briefly list out the differences between TTL, ECL & CMOS logic family. 6 M

4. a) Implement Arithmetic and Logic Unit using Verilog HDL. 10 M

   b) What is a three-state gate and explain each type of three-state gate with truth tables? 6 M

5. a) Write a Verilog HDL code for 4-bit right-to-left shift register using data flow model. 8 M

   b) Draw the state transition tables of JK and T flip flops and implement them in Verilog HDL. 8 M

6. a) With neat circuit diagram explain 2D Decoding in RAM. 10 M

b) Explain the working difference in EPROM and EEPROM. 6 M